Chapter 9

Conclusions

9.1 Future Work

The research presented here on placement and routing algorithms for integrated circuits has spawned a number of open research areas. In this section, we will outline some of those ideas which will lead to algorithmic improvements.

9.1.1 Simulated Annealing

The simulated annealing algorithm has given excellent results while minimizing execution time. In this algorithm, only a single or pairwise exchange of cells is attempted. However, with clustering techniques, large groups of cells may be moved together efficiently. Such a technique promises to dramatically reduce the execution time of simulated annealing.

9.1.2 Macro Cell Placement and Routing

The macro placement algorithm uses a penalty function for overlap resulting in extra terms in the cost function. Extra terms in the cost function reduce the focus from the primary objective, the reduction of wire length. While a statistical method was used to determine the cost function parameters, this operation could be eliminated entirely if compaction was performed after each move. Faster incremental compaction techniques should be investigated to make this a reality.

9.1.3 Mixed Macro and Standard Cell Circuits

In the current mixed macro and standard cell flow, human intervention is required to obtain consistent high quality solutions. It is a complex geometrical problem to determine the optimal row topology given a set of macro cells and a core region. Even the simpler task of discriminating the best topology from a set of alternative is a daunting challenge. Much remains to automate this phase.

9.1.4 Detailed Routing

The area router utilized in this research was gridded and incapable of routing more that two layers. Modern technologies require multiple layer routing. An efficient multi-layer, nongridded, arbitrary design rule area router is today's most critical area of research.

9.1.5 Analog

Charbon et al. introduced a simulated annealing placement algorithm which automatically translated electrical performance specifications into constraints on parasitics [28]. This work should be extended to handle larger circuits and the interactions between analog and digital signals.

9.1.6 Timing

The results of the new pin-pair algorithm are promising. However, more comparisons need to be performed. The biggest obstacle in this area of research is the lack of benchmarks with timing specifications. None of the MCNC benchmark circuits have specified delay bounds. In addition, no logic diagrams are present. While the pin-pair algorithm allows the user to make the circuit as fast as possible without pre-specified targets, a set of specifications will make area trade-off studies viable. The addition of public domain circuits with timing specifications will greatly increase the knowledge in this area.

9.1.7 Global Routing

A lower bound on the time complexity for the minimum spanning tree algorithm on a complete graph is $O\left(N^2 \right)$ where N is the number of nodes. The minimum spanning tree forms the basis for the creation of Steiner trees. For nets with many nodes, this step dominates the execution time. In this case, the minimum spanning tree is not required; a near-optimal solution will suffice. A simple divide-and-conquer method should eliminate the problem.

Another time consuming step of the algorithm is maze routing. While the time complexity is $O\left(N \log N\right)$ (where N is the number of nodes), the constant associated with the maze router dominates the run time. For this reason, an incremental maze approach should be developed which reduces the space and time required.

9.1.8 System Issues

Several new methods have been developed to increase the productivity of the programmer and to reduce the number of errors. Recently, the CWEB system has become available to document and develop *C* programs. Software maintenance of the TimberWolf package should be easier with such a system.

The TimberWolf system mimics object oriented programming through the use of static variables. The unavailability of a standard *C++* on common workstations has limited our use of this language. The implementation of the system in *C++* should shrink the amount of code and increase reliability.

9.2 Summary

In this thesis, computer algorithms for the design of electronic integrated circuits have been presented. Computer-aided design tools which reduce the time of the physical design phase were discussed. Algorithms for all phases of the physical design process were introduced including partitioning, floorplanning, global routing, detailed routing, and compaction. The algorithms may be applied to digital and analog circuits alike because both timing and analog constraints are incorporated. In addition, we have developed the TimberWolf system, a practical implementation of the algorithms. This system has consistently outperformed competing methods over a large set of benchmark circuits. This work presented many algorithmic enhancements to the state of the art. We now review the contributions of this work.

We have presented a new simulated annealing algorithm which is based on a theoretically derived annealing schedule. The quality of the results produced by the new annealing schedule are comparable to Lam's schedule which is statistically optimal with respect to execution time. This algorithm is the basis for the placement and partitioning algorithms presented in this thesis. Our new approach generates a fixed number of moves for a circuit of a given size, and therefore, the number of iterations is known *a priori*.

We have presented a new simulated-annealing-based macro cell layout program which features new methods for statistical wiring estimation, placement refinement, and detailed routing. In particular, we developed a new statistical wire estimation algorithm which reduces the amount of unused routing area. Also, a new placement refinement method was developed for rectilinear cells which spaces the cells at density avoiding the need for post-routing compaction. This method uses previously generated constraints to maintain the topology. A new detailed routing method has been developed which avoids the classically difficult problem of defining channels for detailed routing, and in addition, avoids the

equally difficult problem of defining a routing order for the defined channels. We have obtained the best result for the *ami33* benchmark circuit.

A new fully automatic placement and routing system has been developed for mixed macro/standard cell designs. The system uses a simple yet effective X graphics interface to allow user interaction if desired. At both the standard cell and macro cell level, placement is driven by timing constraints. Based on the results of floorplanning, a new robust method for generating the standard cell row topology has been developed. The floorplanner handles cells of any rectilinear shape and accurately estimates the area necessary for routing.

We have presented a new general net classification scheme for eliminating crosstalk between signals. This has application in the placement of designs containing both analog and digital circuitry.

We have presented six algorithms for controlling the electrical performance of an integrated circuit. A novel pin-pair algorithm controls the time delay without the need for user path specification. The algorithm has optimal time complexity. Using this algorithm, we presented results for the MCNC benchmark circuit *fract*. This is the first report of timing results for any benchmark circuit. The algorithm was able increase the speed of the chip by 34% at an area cost of only 2.5%.

We have presented a new generalized row-based global router suitable for standard cell, gate-array, sea-of-gates, and FPGAs. It is the first row-based global router to explicitly minimize chip area. The global router uses adaptive Steiner trees to accomplish this task. Results were vastly improved over typical minimum wire length Steiner trees. This global router automatically adapts to technologies. In addition, optimal feedthrough placement is accomplished using linear assignment. Throughout the algorithm, timing constraints are taken into account. Furthermore, a unique vertical constraint minimization step

eases the task of LEA (left-edge algorithm) channel routers. Finally, it has been shown that this global router outperforms other global routers for all MCNC circuits tested.

We presented a systematic approach to implementation and testing of a large software system. Software reliability techniques have drastically reduced the number of errors in the system.

The arguments and data presented herein only touch the surface of the dynamic field of electrical engineering. A reflection of a rapidly changing technological environment, advances in our study are seemingly infinite. Clearly, there is much work ahead of us.